RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2816

PATENT APPLICATION
Docket No. 1482-177

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Barrie Gilbert

Serial No.: 10/766,514 Examiner: Minh T. Nguyen

Filed: January 27, 2004 Group Art Unit: 2816

For: SQUARING CELLS AND MULTIPLIERS USING SUMMED EXPONENTIALS

Dated: October 2, 2006 Confirmation No.: 2219

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Commissioner for Patents
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RESPONSE TO FINAL REJECTION UNDER 37 CFR 1.116

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	25	25	0	x $50 =	$ 0
Independent Claims	9	9	0	x $200 =	$ 0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					$ 0

Any deficiency or overpayment should be charged or credited to deposit acct. no. 13-1703.

This communication is responsive to the Office Action dated July 31, 2006.

A listing of the CLAIMS begins on page 2.

REMARKS begin on page 9.

CLAIMS

1. (Cancelled)

2. (Cancelled)

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Cancelled)

9. (Cancelled)

10. (Cancelled)

11. (Cancelled)

12. (Previously presented) A squaring cell comprising:

a first sub-exponential current generator for generating a first current responsive to an input signal; and

a second sub-exponential current generator for generating a second current responsive to the input signal;

wherein the first and second exponential current generators are coupled together to combine the first and second currents.

13. (Previously presented) A squaring cell according to claim 12 wherein each of the sub-exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack.

14. (Previously presented) A squaring cell according to claim 12 wherein each of the sub-exponential current generators includes a back-bias component.

15. (Previously presented) A method for squaring a signal comprising:

generating a first current which varies sub-exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies sub-exponentially responsive to the signal such that the second current decreases when the signal increases; and

combining the first and second currents.

16. (Previously presented) A method according to claim 15 further comprising adding a back-bias effect to the first and second currents.

17. (Previously presented) A method for squaring a signal comprising:

generating a first current which varies exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies exponentially responsive to the signal such that the second current decreases when the signal increases;

combining the first and second currents; and

scaling the first and second currents responsive to a control signal while generating and combining the first and second currents.

18. (Previously presented) A method according to claim 17 further comprising adding a back-bias effect to the first and second currents.

19. (Previously presented) A method for squaring a signal comprising:

generating a first current which varies exponentially responsive to the signal such that the first current increases when the signal increases;

generating a second current which varies exponentially responsive to the signal such that the second current decreases when the signal increases;

combining the first and second currents; and

altering the first and second currents so as to provide sub-exponential functions.

20. (Previously presented) A method according to claim 19 further comprising adding a back-bias effect to the first and second currents.

21. (Previously presented) A multiplier comprising:

a first sub-exponential current generator for generating a first current responsive to a first input signal and a second input signal;

a second sub-exponential current generator for generating a second current responsive to a third input signal and a fourth input signal;

a third sub-exponential current generator for generating a third current responsive to the first input signal and the fourth input signal; and

a fourth sub-exponential current generator for generating a fourth current responsive to the third input signal and the second input signal;

wherein the first and second sub-exponential current generators are coupled together to combine the first and second currents; and

wherein the third and fourth sub-exponential current generators are coupled together to combine the third and fourth currents.

22. (Previously presented) A multiplier according to claim 21 wherein each of the sub-exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack.

23. (Previously presented) A multiplier according to claim 21 wherein each of the sub-exponential current generators includes a back-bias component.

24. (Previously presented) A method for multiplying a first signal and a second signal, wherein the first input signal is the difference between a first signal and a third signal, and the second input signal is the difference between a second signal and a fourth signal, the method comprising:

generating a first current which varies sub-exponentially responsive to the first signal and the second signal;

generating a second current which varies sub-exponentially responsive to the third signal and the fourth signal;

generating a third current which varies sub-exponentially responsive to the fourth signal and the first signal;

generating a fourth current which varies sub-exponentially responsive to the second signal and the third signal;

combining the first and second currents; and

combining the third and fourth currents.

25. (Previously presented) A method according to claim 24 wherein:

combining the first and second currents includes summing the first and second currents; and

combining the third and fourth currents includes summing the third and fourth currents.

26. (Previously presented) A method according to claim 24 further including scaling the first, second, third, and fourth currents responsive to a control signal while generating and combining the currents.

27. (Previously presented) A method according to claim 24 further comprising adding a back-bias effect to the first, second, third and fourth currents.

28. (Previously presented) A squaring cell comprising:

a first exponential current generator for generating a first current responsive to an input signal; and

a second exponential current generator for generating a second current responsive to the input signal;

wherein the first and second exponential current generators are coupled together to combine the first and second currents; and

wherein each of the exponential current generators includes:

a current source;

first and second junctions coupled in series between a first input terminal and the current source;

third and fourth junctions coupled in series between a second input terminal and a node;

a fifth junction coupled between the current source and the node; and

a resistor coupled between the node and the current source.

29. (Previously presented) A squaring cell according to claim 28 wherein each of the exponential current generators further includes a second resistor coupled between the third and fourth junctions.

30. (Previously presented) A squaring cell comprising:

a first exponential current generator for generating a first current responsive to an input signal; and

a second exponential current generator for generating a second current responsive to the input signal;

wherein the first and second exponential current generators are coupled together to combine the first and second currents;

wherein each of the exponential current generators includes:

a constant current stack coupled to a first input terminal; and

a variable current stack coupled to a second input terminal and the constant current stack; and

wherein each constant current stack comprises a resistor arranged to reduce the standing current through the stack.

31. (Previously presented) A squaring cell comprising:

a first exponential current generator for generating a first current responsive to an input signal; and

a second exponential current generator for generating a second current responsive to the input signal;

wherein the first and second exponential current generators are coupled together to combine the first and second currents; and

wherein each of the exponential current generators includes:

a first transistor of a first polarity having a base coupled to a first input terminal for receiving a first side of the input signal;

a second transistor of a second polarity having an emitter coupled to an emitter of the first transistor, a base, and a collector coupled to a node;

a current source coupled to the base of the second transistor;

a third transistor of the first polarity having a base coupled to a second input terminal for receiving a second side of the input signal;

a fourth transistor of the second polarity having an emitter coupled to an emitter of the third transistor, and a base coupled to the node; and

a resistor coupled between the node and the current source.

32. (Previously presented) A squaring cell according to claim 12 wherein the first and second currents comprise substantially sub-exponential currents.

33. (Previously presented) A method according to claim 17 wherein the first and second currents vary substantially sub-exponentially.

34. (Previously presented) A method according to claim 19 wherein the first and second currents vary substantially sub-exponentially.

35. (Previously presented) A multiplier according to claim 21 wherein the first, second, third and fourth currents comprise substantially sub-exponential currents.

36. (Previously presented) A method according to claim 24 wherein the first, second, third and fourth currents vary substantially sub-exponentially.

REMARKS

Claims Rejections Under 35 U.S.C. §102

Claims 12-13, 15, 19, 21-22 and 24-25 are rejected under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 5,909,136 issued to Kimura ("Kimura"). Applicant traverses this rejection.

Arguments From Previous Office Action

Claim 12 recites a squaring cell having two sub-exponential current generators. A sub-exponential current generator differs from a true exponential current generator in that it produces a current having an output function that is deliberately "softened" to result in an output that deviates from an ideal exponential function. (Page 19, lines 12-16.) Purposely softening the exponential functions of the current generators may cause the combined output to more closely approximate an ideal square law. (Page 19, lines 16-18.)

The Examiner argues that Kimura discloses sub-exponential current generators because the exponential function set forth in equation 17 (col. 8, line 18) is based on an approximation. Specifically, the Examiner points to Kimura's assumption, while deriving equation 17, that the DC common-base current gain factor α_F for a transistor is equal to 1, when in practice, α_F is typically equal to 0.98-0.99 for a transistor made with ordinary semiconductor device manufacturing processes. (Col. 8, lines 3-6.)

However, the Examiner has failed to show how, if at all, this approximation affects the exponential relationship. There is no argument or evidence as to whether an α_F that is not unity (not equal to one) would soften the exponential function (which *would* create a sub-exponential function), sharpen the exponential function (which would create something that might be deemed a super-exponential function rather than sub-exponential), have some other effect, or have no effect at all.

In essence, the Examiner is arguing that Kimura inherently discloses a sub-exponential current generator. But in relying upon a theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the prior art. MPEP 2112. Since the Examiner has not shown how a sub-exponential current generator necessarily flows from the teachings of Kimura, the rejection of claim 12 is not properly supported.

In response to Applicant's arguments filed in the Appeal Brief, the Examiner alleges that Kimura teaches that the transistors used in the exponential current generators do not have exactly the same geometry, and therefore, the current generators do not generate ideal exponential functions. This assertion, however, is directly contrary to Kimura's explicit statement that the transistors have matching characteristics. ("The characteristics of transistors Q1-Q4 are essentially identical." Column 6, lines 57-58. See also column 7, lines 39-40 and column 7, lines 62-63.) Even assuming, for the sake of argument, that the transistors are not perfectly matched, the Examiner has not established how, if at all, this would affect the exponential relationship.

Arguments In Final Office Action

In response to Applicant's prior arguments, the Examiner now alleges in the Final Office Action that $I_C = \alpha_F * I_E$, and therefore, the current at the emitters of Q9 and Q14 must be softened because α_F is always less then 1 in a real transistor, and therefore, I_C is always less than I_E.

However, the fact that I_C is always less than I_E does not say anything about the shape of the output function, i.e., whether the exponential function is softened or not. To this end, Applicant provides the following analysis of Kimura's teachings as they would be understood by one of ordinary skill in the art.

Kimura, in Fig. 5, discloses a squaring circuit using bipolar transistors (column 6, lines 54-57). The circuit has two differential pairs of transistors, Q1-Q2 and Q3-Q4. The differential output ΔIc of the first differential pair Q1-Q2 is given by equation 14. Also, equations 15 and 16 set forth the relationship between different currents in the differential pair. Kimura states that if the DC common base current gain $\alpha_F = 1$, then equations 14, 15 and 16 may be combined to obtain equation 17, which discloses an exponential current generator. However, Kimura further states that α_F may in practice be in the range of 0.98-0.99. To better understand the effects of α_F on I_{C2}, Kimura's equations 15 and 16 may be substituted into equation 14, and the well-known relationship $\tanh(x) = \frac{\exp^x - \exp^x}{\exp^x + \exp^x} = \frac{\exp^{2x} - 1}{\exp^{2x} + 1}$ may be used to obtain:

$$I_0 - Ic_2 = \alpha_F (I_0 + Ic_2) \frac{\exp^{2\frac{V_i}{2V_T}} - 1}{\exp^{2\frac{V_i}{2V_T}} + 1} \qquad \text{Eq. A}$$

which may be rearranged as follows:

$$I_0\left(1-\alpha_F\frac{\exp^{\frac{V_i}{V_T}}-1}{\exp^{\frac{V_i}{V_T}}+1}\right)=Ic_2\left(1+\alpha_F\frac{\exp^{\frac{V_i}{V_T}}-1}{\exp^{\frac{V_i}{V_T}}+1}\right) \qquad \text{Eq. B}$$

$$Ic_2\left(\exp^{\frac{Vi}{V_T}}+1+\alpha_F\left(\exp^{\frac{V_i}{V_T}}-1\right)\right)=I_0\left(\exp^{\frac{V_i}{V_T}}+1-\alpha_F\left(\exp^{\frac{V_i}{V_T}}-1\right)\right) \qquad \text{Eq. C}$$

$$Ic_2=I_o\frac{\exp^{\frac{V_i}{V_T}}+1-\alpha_F\left(\exp^{\frac{V_i}{V_T}}-1\right)}{\exp^{\frac{V_i}{V_T}}+1+\alpha_F\left(\exp^{\frac{V_i}{V_T}}-1\right)} \qquad \text{Eq. D}$$

Equation D illustrates how Kimura's I_{C2} is related to α_F. For α_F =1, the above equation is equivalent to equation 17 of Kimura, which is a pure exponential function. However, for other values of α_F, the behavior of I_{C2} deviates from a pure exponential function as shown in the following table which illustrates the output I_{C2} for various values of input voltage Vi for three different values of α_F (0.98, 0.99 and 1). A normalized value of I_0 =1 is assumed.

Vi / V_T	Ic2 (for α_F = 0.98)	Ic2 (for α_F = 0.99)	Ic2 (for α_F = 1.0)
0	1	1	1
0.25	0.782744	0.78077	0.778801
0.5	0.612877	0.609697	0.606531
0.75	0.480176	0.476261	0.472367
1	0.376581	0.372216	0.367879
1.25	0.29575	0.291111	0.286505
1.5	0.232707	0.2279	0.22313
1.75	0.183553	0.178643	0.173774
2	0.145238	0.140265	0.135335
2.25	0.115377	0.110366	0.105399
2.5	0.09211	0.087074	0.082085
2.75	0.073981	0.068931	0.063928
3	0.059858	0.054798	0.049787
3.25	0.048856	0.043791	0.038774

From the table it is apparent that as Vi/V_T increases, the value of the current I_{C2} increases more rapidly when $\alpha_F = 0.99$ (or $\alpha_F = 0.98$), than when $\alpha_F = 1$. Thus, for $\alpha_F < 1.0$, the current I_{C2} exhibits a steeper slope that sharpens the exponential function, i.e., it exhibits what can be described as a ***super***-exponential function rather than a ***sub***-exponential function as recited in claim 1.

For at least this reason, claim 12 is not anticipated by Kimura, nor is claim 13 which recites addition features that are not taught or suggested by the prior art.

Claims 15, 19, 21, and 24 also include limitations relating to sub-exponential current functions. For at least the reasons discussed above with respect to claim 12, these claims are not anticipated by Kimura, nor are claims 22 and 25 which recite addition features that are not taught or suggested by the prior art.

Claims Rejections Under 35 U.S.C. §103

Claims 17 and 26 are rejected under 35 U.S.C. §102(a) as being unpatentable over Kimura in view of U.S. Patent No. 6,173,346 issued to Wallach, et al. ("Wallach"). Applicant traverses this rejection.

Arguments From Previous Office Action

Claim 17 recites scaling the first and second currents while generating and combining the first and second currents. In other words, the scaling is performed while the circuit is in operation. In the embodiment of Fig. 20, scaling may be accomplished by varying the bias currents I_0 in response to a control signal as explained in the specification at page 20, lines 24-27. The specification further discloses at page 20, lines 25-28 that scaling the first and second currents while the circuit is in operation may provide the benefit of allowing squaring and weighting functions to be performed simultaneously, e.g., by using a weighting signal as the control signal.

Kimura discloses varying certain bias signals by programming them in a manner that would have the effect of scaling the first and second currents. (Col. 8, lines 57-58.) However, the Examiner acknowledges that Kimura does not disclose scaling the bias signals while the circuit is in operation. Kimura only mentions that programming the bias signals allows for easy circuit design and integration in large scale integration (LSI). (Col. 8, lines 58-62.)

From this, the Examiner makes the analytical leap that it would have been obvious to perform the scaling operation while the circuit is in operation because it would be desirable to do so because the circuit does not need to be powered down. In support of this leap, the Examiner cites Wallach as teaching the desirability of adding or replacing the functionality of a circuit using programming without powering down the system. There are several problems with this argument.

First, Wallach is not pertinent art. Claim 17 recites a method which, in view of the specification, is directed to the realm of analog signal processing. The specification discusses numerous embodiments of transistor-level circuits in terms of signals, currents, squaring, multiplying, etc., as analog concepts. In contrast, Wallach relates to "I/O adaptors in computer systems" (col. 5, lines 40-41) which are digital systems. Thus, Wallach would not be considered reasonably pertinent to the particular problem with which the inventor was involved.

Second, as best understood by Applicant, the Examiner's arguments regarding not needing to "power down the system" seem to contemplate a notion of discrete operating modes where the system switches between different fixed operating parameters. However, as disclosed in Applicant's specification, scaling the currents while the circuit is in operation may enable not just a change in modes, but rather the integration of two functions into one operation, e.g., allowing squaring and weighting functions to be performed simultaneously. None of the cited references provide the suggestion or motivation for such a modification to the prior art.

Third, claim 17 recites scaling the first and second currents responsive to a control signal. In one embodiment, such a control signal may be a weighting signal as discussed above. The examiner alleges that Kimura discloses a current source I_0 that can be scaled in response to a control signal, but identifies no such control signal, nor any suggestion or motivation to scale anything in response to a control signal. Kimura teaches that I_0 is a constant current source (col. 8, line 23), and at most may be a programmable parameter (col. 8, line 59) which allows easy circuit design and is suitable for LSI. But these teachings relate to varying parameters at the time the circuit is designed and manufactured, not while it is operating, and not in response to a control signal.

Finally, not only is the combination of Kimura and Wallach untenable, but it is based on an impermissible hindsight reconstruction using the Applicant's disclosure as a roadmap to achieve the claimed invention. The Examiner has not identified any motivation or suggestion in

Kimura, Wallach, or any other reference, to scale sub-exponential currents while the circuit is in operation. Thus, a *prima facie* case of obviousness has not been established for claim 17.

Arguments In Final Office Action

Regarding Applicant's (first) argument that Wallach is not pertinent art, the Examiner responds that Wallach relates to electronic circuits and is therefore pertinent. However, "electronic circuits" is an overbroad characterization of the subject matter. In evaluating whether a reference is reasonably pertinent to the particular problem with which the inventor was involved, the structure and function of the claimed subject matter should be compared to that of the reference. MPEP 2141.01(a)(II). Claim 17 recites generating currents, and its function is to provide the mathematical square of two analog signals. Wallach does not disclose any electrical currents, and the function of Wallach's technology relates to hot-swapping I/O adaptors in computer systems. Wallach does not disclose the manipulation of any analog signal, much less the squaring of an analog signal as recited in claim 17. Thus, the structure and function of Wallach is so different from that of claim 17, that Wallach cannot be considered reasonable pertinent.

The Examiner tries to characterize the problem as modifying a circuit *parameter* while in operation. But the method recited in claim 17 does not just modify a parameter, it enables an entirely new mode of operation and additional functionality by allowing a squaring cell to perform squaring and weighting functions simultaneously, in response to a control signal that operates as an additional input, as disclosed in the specification at page 20, lines 25-28. Wallach discloses no such functionality that a person of ordinary skill in the art would have turned to for guidance.

Regarding Applicant's (second) argument that the method recited in claim 17 enables squaring and weighting functions to be performed simultaneously, the Examiner argues that this benefit is not recited in the claim. The Examiner has not cited, and Applicant is unaware of, any authority for the proposition that a potentially beneficial result must be recited in the claim.

Regarding Applicant's (third) argument that Wallach does not identify a control signal and only teaches changing parameters during design or manufacture, the Examiner responds that (1) parameters that are applied during design or manufacture would be called design parameters, and (2) electrically programmable parameters read to an electrical signal. As best understood by

Applicant, the essence of this argument is that, if something can be programmed, then it can be programmed in response to a signal. But this still fails to identify all of the elements of claim 17 in the cited references, as well as any motivation or suggestion to modify or combine the references.

Regarding Applicant's (fourth or final) argument that the combination of Kimura and Wallach is untenable and based on an impermissible hindsight reconstruction, the Examiner responds that Wallach teaches adjustment of a circuit while in operation, and Kimura teaches adjusting exponential currents in general. In essence, the Examiner seems to be arguing that Wallach teaches that, if something can be adjusted, then it can be adjusted during operation. This is an unreasonably broad interpretation of Wallach, and it ignores the rule that a claim must be interpreted as a whole. Claim 17 recites a method for squaring a signal by generating and combining two currents, and simultaneously scaling the currents in response to a control signal. Simultaneously scaling the currents in response to a control signal does not "adjust" a circuit as alleged by the Examiner, it enables an entirely new mode of operation and additional functionality by allowing a squaring cell to perform squaring and weighting functions simultaneously, where the control signal serves as an additional input, as discussed above.

For at lest these reasons, a *prima facie* case of obviousness has not been established for claim 17. Similar arguments apply to claim 26.

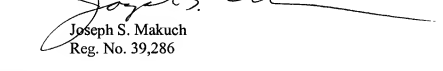
Conclusion

Applicant requests reconsideration in view of the foregoing remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Customer No. 20575

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



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